

FIG. 1 PRIOR ART

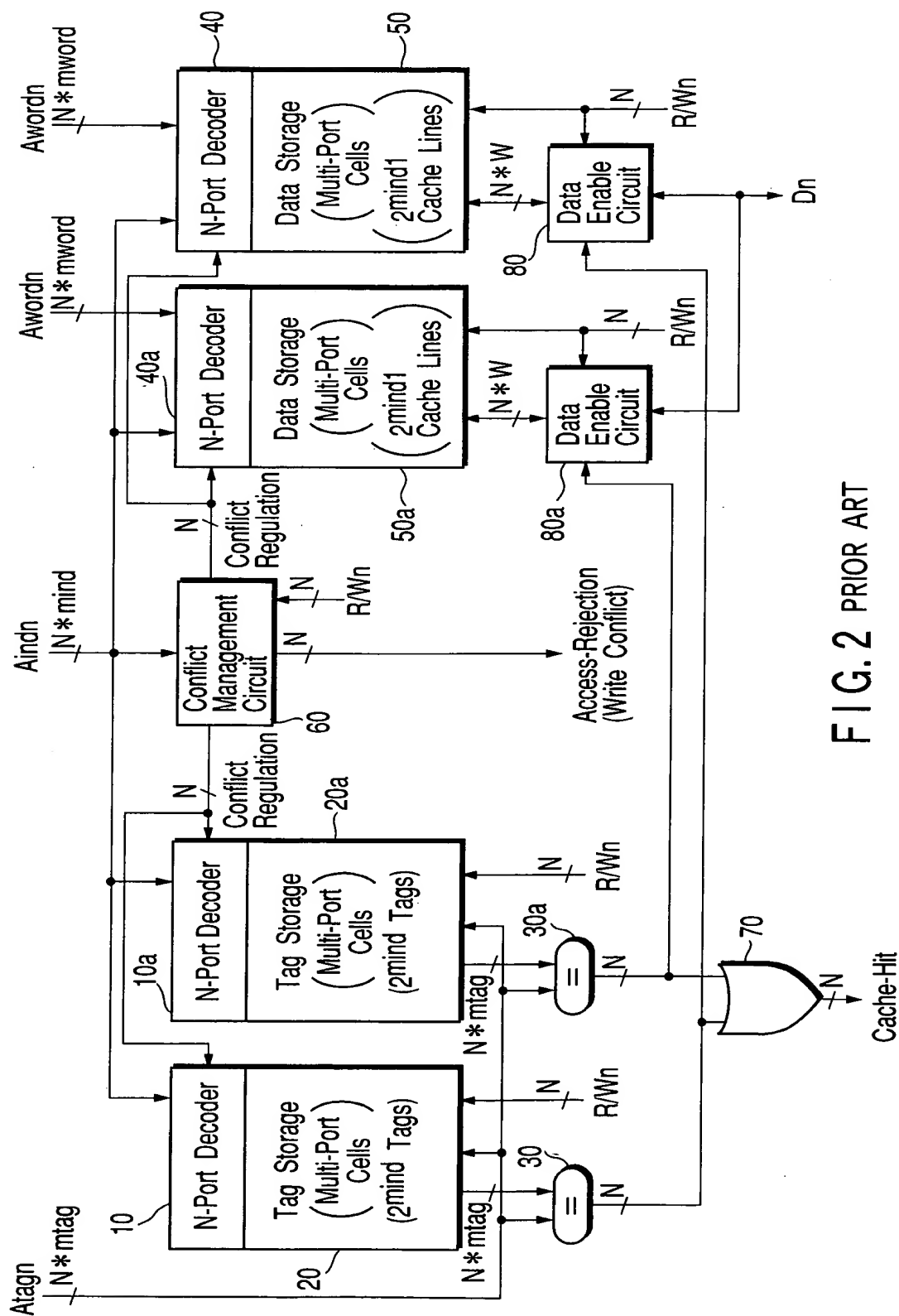


FIG. 2 PRIOR ART

Atag (mtag bits)	Aind (mind bits)	Aword (mword bits)	Abyte (mbyte bits)
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FIG. 3 PRIOR ART

General Case

Atag (mtag bits)	Aind2 (mind2 bits)	Aind1 (mind1 bits)	Aword (mword bits)	Abyte (mbyte bits)
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FIG. 5A

512Kbit, Direct-Mapped, 8-Port Cache, 4 Word Per Line Cache Memory  
(32Bit Addresss Space, 32bit Wordlength)

	Atag (bits)	Aind2 (bits)	Aind1 (bits)	Aword (bits)	Abyte (bits)
Conventinal Multi-Port Cache Memory	16	12		2	2
Multi-Port Cache Memory according to the invention	16	7 Data-Storage: 128 blocks each 4Kbit Tag-storage: 128 blocks each 480bit	5	2	2

FIG. 5B

FIG. 5B

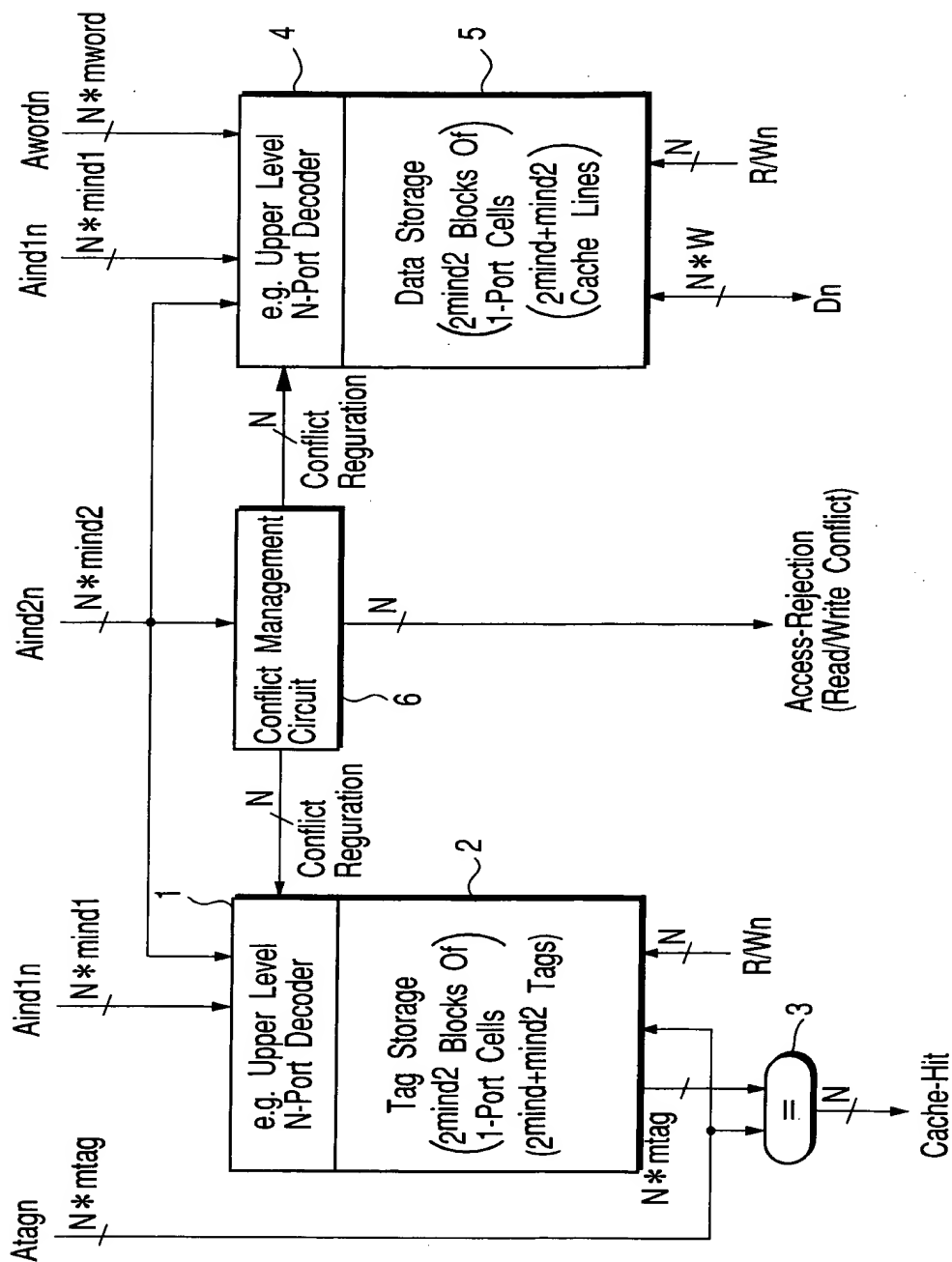
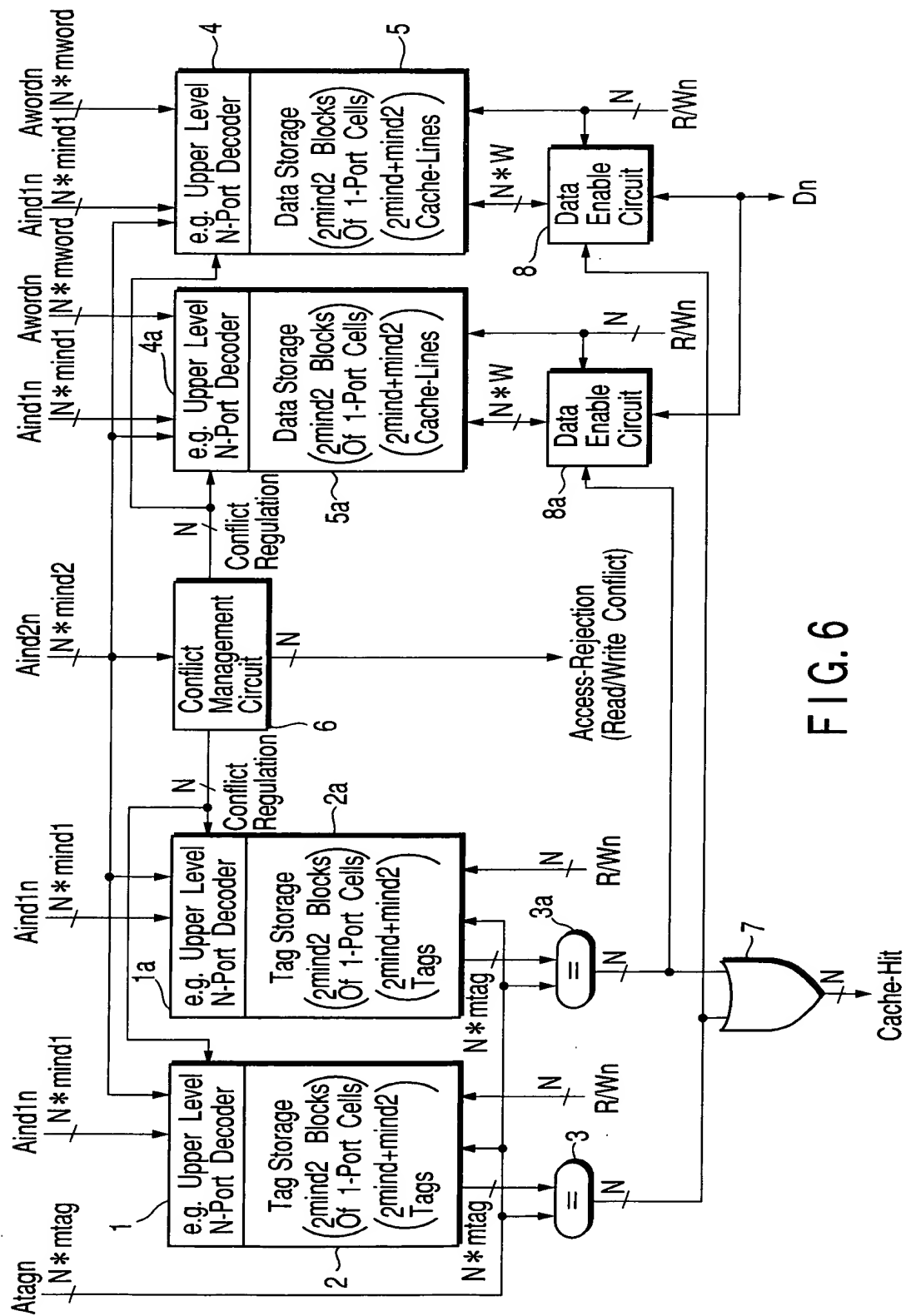


FIG. 4



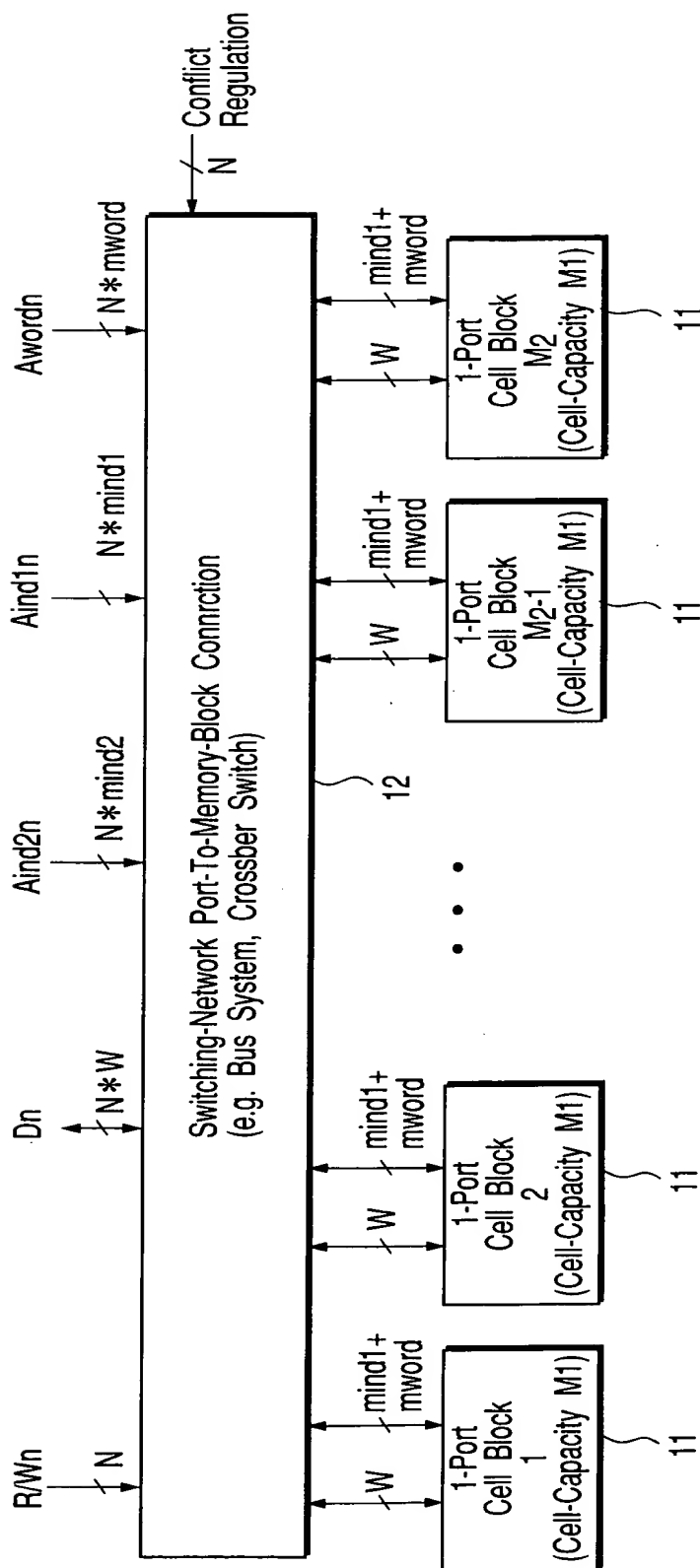


FIG.7

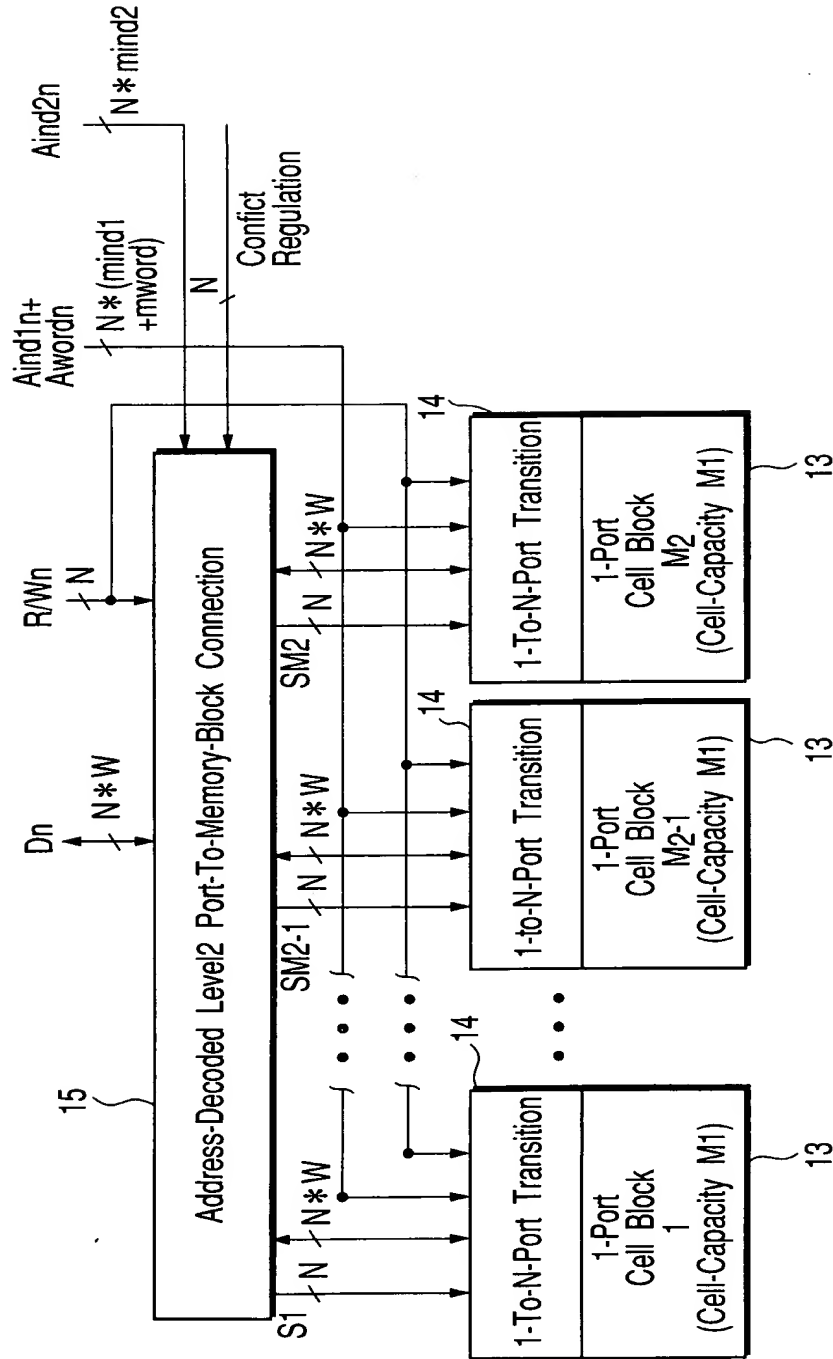


FIG. 8

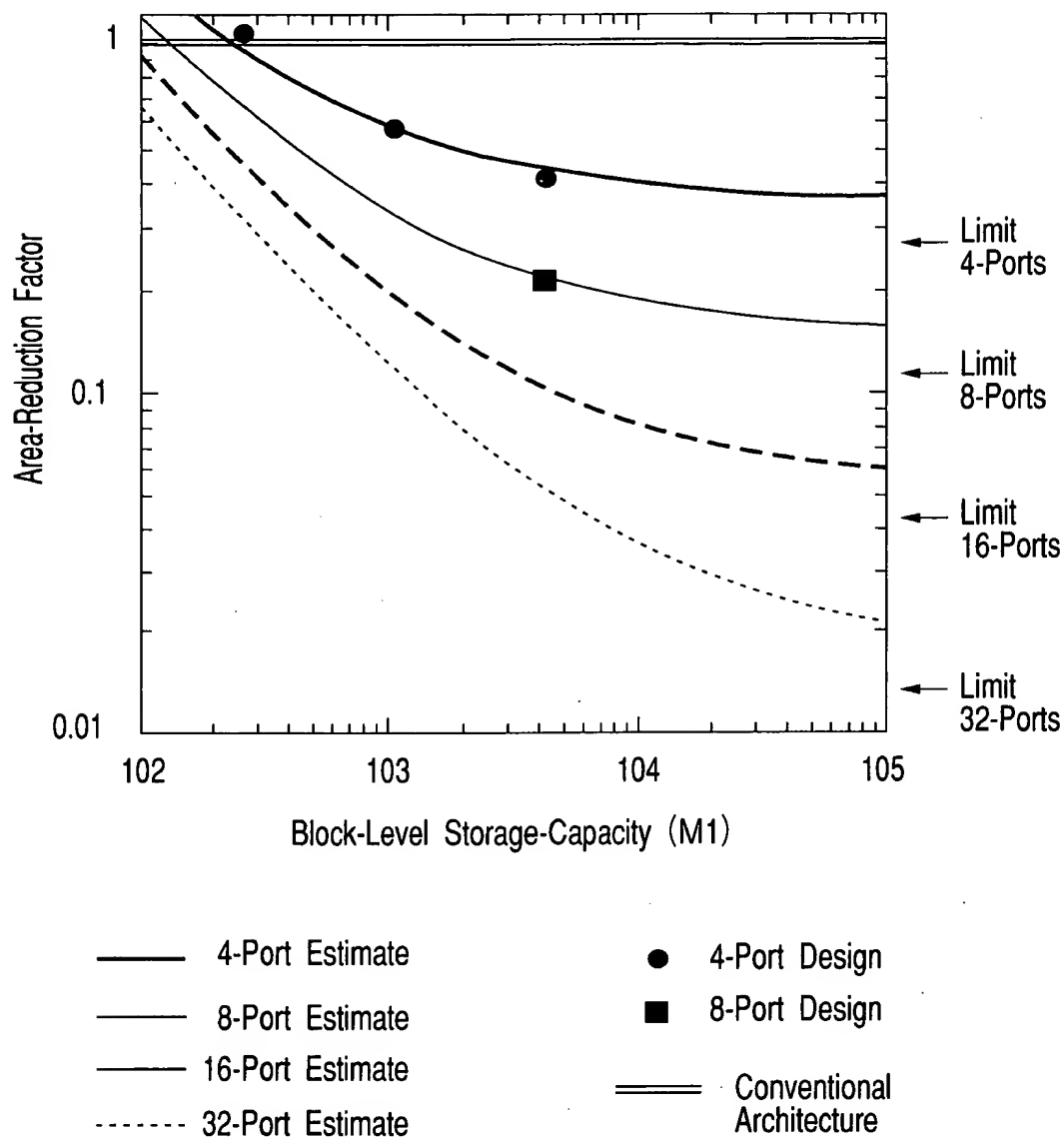


FIG. 9



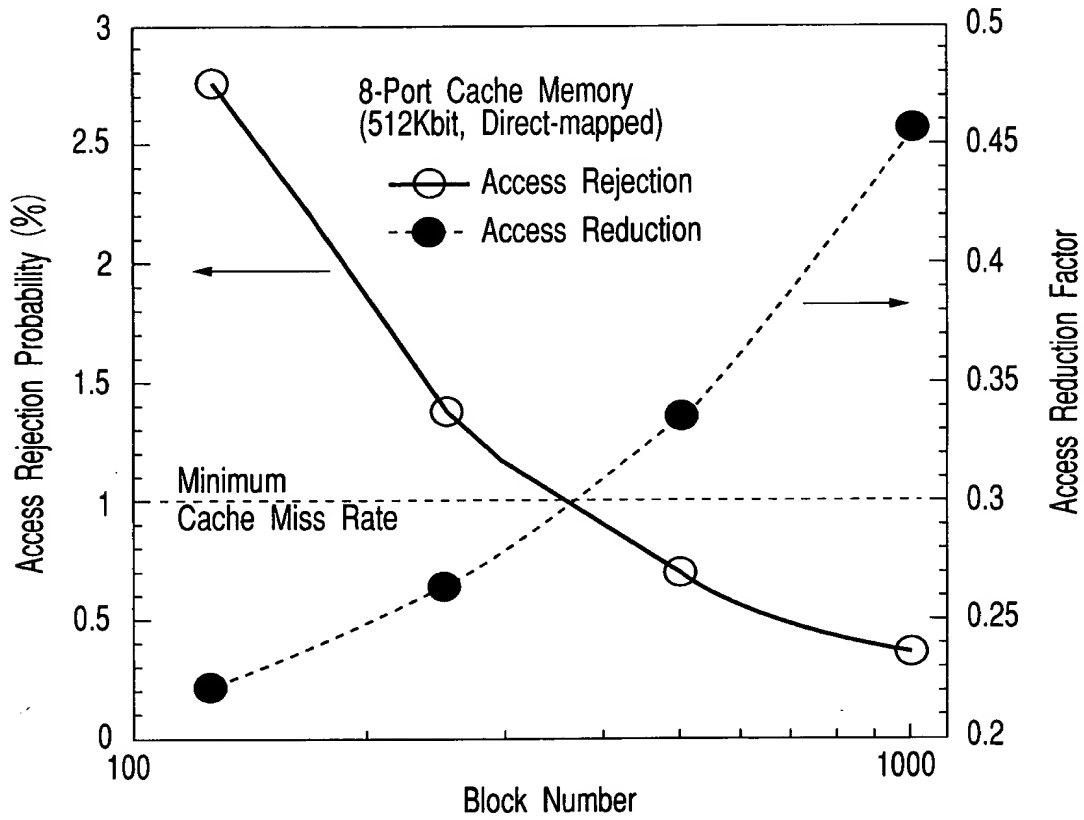


FIG. 10